RAAK

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi & Affiliated to Pondicherry University)

VALUE ADDED COURSES

2018-2019

Department of Electrical & Electronics Engineering

18EE01-Embedded C for Electrical Engineering

MARK SHEET

Sl. No	Register Number	Student Name	MARKS
1	17TE3101	GUNALAN.M	96

HOD

PRINCIPAL

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

RAAK

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi & Affiliated to Pondicherry University)

VALUE ADDED COURSES

2018-2019

Department of Electrical and Electronics Engineering

18EE01-Embedded C for Electrical Engineering

NAME:

CLASS:

DATE:

1. Which memory storage is widely used in PCs and Embedded Systems?

a) EEPROM b) Flash memory

c) SRAM d) DRAM

Answer: d

2. How is the protection and security for an embedded system made?

a) Security chips b) Memory disk security

c) IPR d) OTP

Answer: c

3. Which of the following task swapping method is a better choice in the embedded systems design?

a) time slice b) RMS

c) cooperative multitasking d) pre-emptive

Answer: d

Explanation: The pre-emptive method of task swapping is the first choice for embedded system design because of its better system response.

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

4. Which type of memory is suitable for low volume production of embedded systems?

a) Non-volatile
b) RAM
c) Volatile
d) ROM

Answer: a

5. Which activity is concerned with identifying the task at the final embedded systems?

a) scheduling
b) task-level concurrency management
c) high-level transformation
d) compilation

Answer: b

6. Which level simulates the algorithms that are used within the embedded systems?

a) algorithmic level
b) switch level
c) gate level
d) circuit level

Answer: a

7. How an embedded system communicate with the outside world?

a) Memory
b) Output
c) Peripherals
d) Input

Answer: c

8. Which of the following helps in reducing the energy consumption of the embedded system?

a) emulator
b) debugger
c) simulator
d) compilers

Answer: d

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

9. What is the purpose of memory refresh register of Z80?

a) To control on-chip SRAM
b) To control on-chip DRAM
c) To clear cache
d) To control ROM

Answer: b

10. What does MESI stand for?

a) modified exclusive system input
b) modifies embedded shared invalid
c) modified exclusive shared invalid
d) modified exclusive stale invalid

Answer: c

11. Which of the following is the pin efficient method of communicating between other devices?

a) memory port
b) peripheral port
c) parallel port
d) serial port

Answer: d

12. Which of the following is a traditional method for emulating the processor?

a) CPU simulator
b) SDS
c) ICE
d) Low-level language simulator

Answer: c

13. Which of the following unit protects the memory?

a) memory management unit
b) peripheral unit
c) execution unit
d) bus interface unit

Answer: a

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

14. Identify the standard software components that can be reused in an embedded system design?

a) memory
b) application software
c) application manager
d) operating system

Answer: d

15. What does ICE stand for?

a) in-circuit EPOM
b) in-code emulation
c) in-circuit emulation
d) in-code EPROM

Answer: c

16. Who proposed the first power model?

a) Tiwari
b) Russell and Jacome
c) Russell
d) Jacome

Answer: a

17. Which of the following offers external chips for memory and peripheral interface circuits?

a) Embedded system
b) Peripheral system
c) Microcontroller
d) Microprocessor

Answer: d

18. What kind of socket does an external EPROM to plugged in for prototyping?

a) Piggyback reset socket
b) Multi-socket
c) Piggyback
d) Single socket

Answer: c

19. Which is the single device capable of providing prototyping support for a range of microcontroller?

a) Umbrella device
b) OTP
c) RAM
d) ROM

Answer: a

20. By which instruction does the switching of registers take place?

a) Register instruction
b) EXX instruction
c) Instruction opcodes
d) AXX instruction

Answer: c

21. Which of the architecture is more complex?

a) MC68040
b) MC68030
c) SPARC
d) 8086

Answer: c

22. Which of the following statements are true for von Neumann architecture?

a) separate bus between the program memory and data memory

b) external bus for program memory and data memory

c) external bus for data memory only

d) shared bus between the program memory and data memory

Answer: d

23. What is approximate data access time of SRAM?

a) 2ns
b) 10ns
c) 60ns
d) 4ns

Answer: d

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

24. Which of the following is a plastic package used primarily for DRAM?

a) Zig-zag
b) DIMM
c) SIMM
d) Dual-in-line

Answer: a

25. Which of the following is the biggest challenge in the cache memory design?

a) coherency
b) memory access
c) size
d) delay

Answer: a

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.,
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road
Sulthanpet Post.
Puducherry - 605 ...

RAAK

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi & Affiliated to Pondicherry University)

VALUE ADDED COURSES

2018-2019

Department of Electrical and Electronics Engineering

18EE01-Embedded C for Electrical Engineering

NAME: GUNALAN.M

CLASS: II / EEE

DATE: 20/08/2018

1. Which memory storage is widely used in PCs and Embedded Systems?
a) EEPROM b) Flash memory
c) SRAM d) DRAM

2. How is the protection and security for an embedded system made?
a) Security chips b) Memory disk security
c) IPR d) OTP

24/25 96%

3. Which of the following task swapping method is a better choice in the embedded systems design?
a) time slice b) RMS
c) cooperative multitasking d) pre-emptive

4. Which type of memory is suitable for low volume production of embedded systems?
a) Non-volatile b) RAM
c) Volatile d) ROM

5. Which activity is concerned with identifying the task at the final embedded systems?
a) scheduling b) task-level concurrency management
c) high-level transformation d) compilation

6. Which level simulates the algorithms that are used within the embedded systems?
a) algorithmic level b) switch level
c) gate level d) circuit level

7. How an embedded system communicate with the outside world?
a) Memory b) Output
c) Peripherals d) Input

8. Which of the following helps in reducing the energy consumption of the embedded system?
a) emulator b) debugger
c) simulator d) compilers

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

9. What is the purpose of memory refresh register of Z80?
a) To control on-chip SRAM
b) To control on-chip DRAM
c) To clear cache
d) To control ROM

10. What does MESI stand for?
a) modified exclusive system input
b) modifies embedded shared invalid
c) modified exclusive shared invalid
d) modified exclusive stale invalid

11. Which of the following is the pin efficient method of communicating between other devices?
a) memory port
b) peripheral port
c) parallel port
d) serial port

12. Which of the following is a traditional method for emulating the processor?
a) CPU simulator
b) SDS
c) ICE
d) Low-level language simulator

13. Which of the following unit protects the memory?
a) memory management unit
b) peripheral unit
c) execution unit
d) bus interface unit

14. Identify the standard software components that can be reused in an embedded system design?
a) memory
b) application software
c) application manager
d) operating system

15. What does ICE stand for?
a) in-circuit EPOM
b) in-code emulation
c) in-circuit emulation
d) in-code EPROM

16. Who proposed the first power model?
a) Tiwari
b) Russell and Jacome
c) Russell
d) Jacome

17. Which of the following offers external chips for memory and peripheral interface circuits?
a) Embedded system
b) Peripheral system
c) Microcontroller
d) Microprocessor

18. What kind of socket does an external EPROM to plugged in for prototyping?
a) Piggyback reset socket
b) Multi-socket
c) Piggyback
d) Single socket

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

19. Which is the single device capable of providing prototyping support for a range of microcontroller?
a) Umbrella device
b) OTP
c) RAM
d) ROM

20. By which instruction does the switching of registers take place?
a) Register instruction
b) EXX instruction
c) Instruction opcodes
d) AXX instruction

21. Which of the architecture is more complex?
a) MC68040
b) MC68030
c) SPARC
d) 8086

22. Which of the following statements are true for von Neumann architecture?
a) separate bus between the program memory and data memory
b) external bus for program memory and data memory
c) external bus for data memory only
d) shared bus between the program memory and data memory

23. What is approximate data access time of SRAM?
a) 2ns
b) 10ns
c) 60ns
d) 4ns

24. Which of the following is a plastic package used primarily for DRAM?
a) Zig-zag
b) DIMM
c) SIMM
d) Dual-in-line

25. Which of the following is the biggest challenge in the cache memory design?
a) coherency
b) memory access
c) size
d) delay

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

RAAK

COLLEGE OF ENGINEERING AND TECHNOLOGY

(Approved by AICTE, New Delhi & Affiliated to Pondicherry University)

VALUE ADDED COURSES

2019-2020

Department of Electricaland Electronics Engineering

19EE01-Modern Optimization Techniques for Electric Power System

NAME: GUNALAN.M

CLASS: III / EEE

DATE: 20/08/2019

1. Single line diagram of which of the following power system is possible?
a) Power system with LG fault
b) Balanced power system
c) Power system with LL fault
d) Power system with LLG fault

24/25

96%

2. A power system will have greater flexibility of operation if they have _____
a) Only Base load plants operating in combination
b) Various types of power plants operating in combination
c) Only Peak load plants operating in combination
d) Only thermal power plants operating in combination

3. Single line diagram does not represents:
a) Ratings of machines
b) Neutral wire of transmission lines
c) Delta connection of transformer winding
d) Star connection of transformerwinding

4. In impedance diagram different power system elements are represented by symbols.
a) False
b) True

5. In combined operation of several power plants the reserve capacity requirement is reduced.
a) False
b) True

6. For a given power system, its zero and maximum regulation will occur at the impedance angle of
a) 45
b) 60
c) 35
d) 50

7. A 200 bus power system has 160 PQ bus. For achieving a load flow solution by N-R in polar coordinates, the minimum number of simultaneous equation to be solved is
a) 359
b) 334
c) 358
d) 345

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

8. A 50 bus power system Ybus has 80% sparsity. The total number of transmission lines will be _____
a) 225
b) 563
c) 345
d) 456

9. The given graph is the depiction of _____ on a large power system network.
a) Three phase motor getting short
b) L-G fault
c) Ratings of machines
d) Any of the mentioned

10. A protection system engineer is planning to provide the complete protection, he can achieve this by _____
a) a two phase fault relays and three earth fault relays
b) a two phase fault relays and two earth fault relays
c) two phase fault relays and three earth fault relays
d) three phase fault relays and two earth fault relays

11. A power system has a maximum load of 15 MW. Annual load factor is 50%. The reserve capacity of plant is _____ if the plant capacity factor is 40%.
a) 8.75 MW
b) 7.75 MW
c) 46.75 MW
d) 8.75 MW

12. The area under the load curve represents _____
a) maximum demand
b) load factor
c) the average load on power system
d) number of units generated

13. If all the sequence voltages at the fault point in a power system are equal, then fault is _____
a) LLG fault
b) Line to Line fault
c) Three phase to ground fault
d) LG fault

14. If the power system network is at $V_s\angle\delta$ and receiving end voltage is $V_r\angle 0$ consisting of the impedance of TL as $(R+j5)\Omega$. For maximum power transfer to the load, the most appropriate value of resistance R should be _____
a) 1.732
b) 3.45
c) 5.2
d) 0.33

15. Voltage regulation in the power system is _____
a) dip in voltage at sending end
b) rise in voltage at sending end
c) rise in voltage at receiving end
d) dip in voltage at receiving end

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

16. Which of the following is not neglected during formation of reactance diagram from impedance diagram?
a) Shunt component of Transformers
b) Static loads
c) Resistance of various power system components
d) Reactance of alternators

17. Which of the following is not a requirement for site selection of hydroelectric power plant?
a) Large catchment area
b) Rocky land
c) Sedimentation
d) Availability of water

18. Which of the following is not an advantage of hydroelectric power plant?
a) no fuel requirement
b) continuous power source
c) low running cost
d) no standby losses

19. Which of the following element of hydroelectric power plant prevents the penstock from water hammer phenomenon?
a) Surge Tank
b) Draft tubes
c) Spillway
d) Valves and Gates

20. Which of the following part of thermal power plant causes maximum energy losses?
a) Alternator
b) Ash and unburnt carbon
c) Boiler
d) Condenser

21. Which of the following are the most widely used condensers in modern thermal power plants?
a) Low level counter flow type jet condenser
b) Parallel flow type jet condenser
c) High level counter flow type jet condenser
d) Surface condensers

22. Which of the following is most suitable fuel for thermal power plant?
a) Bituminous coal
b) Lignite coal
c) Anthracite coal
d) Peat coal

23. Which of the following is most advantageous and most widely method of solid fuel firing?
a) Spreader stoker firing
b) Pulverised fuel firing
c) Underfeed firing
d) Stoker firing

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

24. Which of the following method is used in large modern thermal power plants to heat feed water?

a) Open type heatre is used
b) Surface type hater is used
c) Close type heater is used
d) Steam is directly taken from main turbine and used to eat it feed water

25. Which of the following pollutant causes acid rain?

a) NO_2
b) SO_2
c) CO_2
d) NO

RAAK College of Engineering & Technology

Dr. S. SEENUVASAMURTHI, M.E., Ph.D.
PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

RAAK

COLLEGE OF ENGINEERING & TECHNOLOGY

(Approved by AICTE, New Delhi, Affiliated to Pondicherry University)

NO:1, MUTHUPILLAI PALAYAM ROAD, G.N. PALAYAM, VILLIYANUR, PUDUCHERRY - 605 110

Certificate of Completion

2018-2019

This is to certify that Mr/Ms.....GUNALAN.M.....

Year...II..... Department...EEE..... has successfully Completed the Value added course.

COURSE TITLE: EMBEDDED C FOR ELECTRICAL ENGG.

SCORE: .....96.....

COURSE DURATION: ..9/.8/.2018..to..14./8/.18.

.....

HOD

PRINCIPAL
RAAK College of Engineering & Technology
No.1, Muthupillai Palayam Road,
Sulthanpet Post,
Puducherry - 605 110

PRINCIPAL